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Question Paper Code : 11164

B.E./B.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2026.

Third Semester

Computer Science and Engineering

CS3351 — DIGITAL PRINCIPLES AND COMPUTER ORGANIZATION

(Common to : Computer Science and Design/Computer Science and Engineering
(Artificial Intelligence and Machine Learning)/Computer science and Engineering
(Cyber Security)/Computer and Communication Engineering /Electrical and
Computer Engineering/Artificial Intelligence and Data Science/Computer Science
and Business Systems/Information Technology)

(Regulations 2021)

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Define encoder and decoder.
2. Draw the logic diagram for a half adder and write its Boolean expression.
3. Write the truth table for JK flip-flop.
4. What is a race condition?
5. Write the effective address calculation for Indexed Addressing Mode.
6. Convert the assembly instruction ADD R1, (R2) + into its micro-operations.
7. Define pipelining.
8. A CPU has cache access time = 10 ns and main memory access time = 100 ns. If the cache hit ratio is 0.9, find the effective access time.
9. Define Direct Memory Access (DMA).
10. What is virtual memory?

PART B — (5 × 13 = 65 marks)

11. (a) (i) Explain the simplification of Boolean expressions using Karnaugh maps with a 4-variable example. (7)

- (ii) Simplify the Boolean expression using 4-variable K-map:

$$F(A, B, C, D) = \sum(0, 1, 2, 5, 6, 7, 8, 9, 10, 14). \quad (6)$$

Or

- (b) (i) Describe the design of a 4-bit magnitude comparator using combinational circuits and logic gates. (7)
- (ii) Design a 3-bit even parity generator and checker using XOR gates. (6)
12. (a) Explain the operation and characteristic equations of JK, SR, and D flip-flops.

Or

- (b) Describe the state diagram and state table of a Moore machine that detects the sequence "1011".
13. (a) (i) Discuss the various machine instruction formats with examples. (7)
- (ii) Given memory access time = 500 ns and instruction cycle = 2 μ s, calculate the CPU utilization for a program performing one memory access per instruction. (6)

Or

- (b) (i) Discuss the various addressing modes used in computer instruction sets with examples. (7)
- (ii) An instruction set has 16-bit instructions and 4 addressing modes. Find the number of bits required for opcode and address fields if the processor has 256 memory locations. (6)
14. (a) (i) Explain the steps involved in instruction execution and discuss the design of a control unit. (7)
- (ii) A pipeline has 5 stages with stage times of 100 ns each. Calculate the throughput and speedup for 100 instructions. (6)

Or

- (b) (i) Describe pipelining and explain the problems caused by structural, data, and control hazards. (7)
- (ii) Draw a timing diagram for instruction pipelining showing structural, data, and control hazards. (6)

15. (a) Explain the hierarchical memory structure of a computer and the functioning of cache memory.

Or

- (b) Discuss various I/O interfacing methods and compare programmed I/O, interrupt-driven I/O, and DMA.

PART C — (1 × 15 = 15 marks)

16. (a) (i) Design a simple processor model showing the data path and control unit organization. Explain each block. (8)
- (ii) Design a synchronous counter that counts in the sequence 0, 1, 3, 2 using JK flip-flops. Show all steps. (7)

Or

- (b) (i) Explain how instruction pipelining improves CPU performance. Use a 5-stage pipeline example. (8)
- (ii) Propose a hybrid memory system combining cache, virtual and main memory. Explain how access time and performance are optimized. (7)
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